



Specification for Approval

Customer: _____

Model Name: _____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
<i>Peter</i>	<i>Peng Jun</i>		



Revision Record

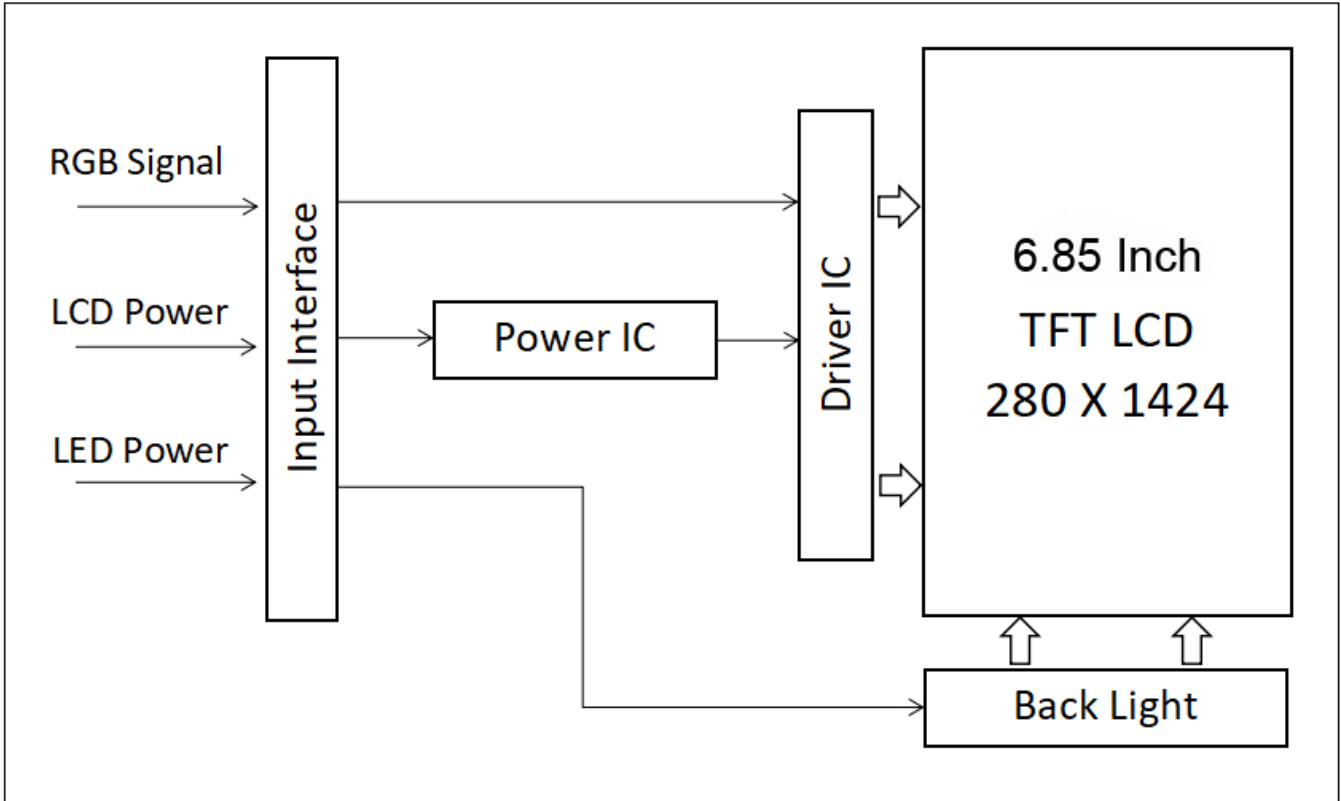
REV NO.	REV DATE	CONTENTS	Note
V0	2024-10-22	NEW ISSUE	

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1. General Description

The LCM 6.85_RGB is a 280 x 3RGB x1424 dots matrix 6.85" TFT LCD module.



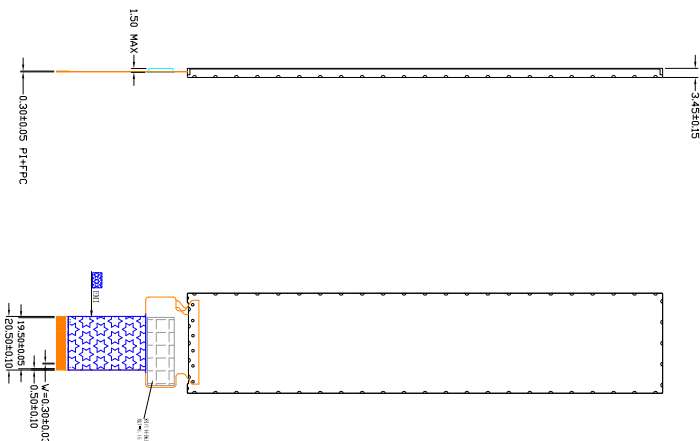
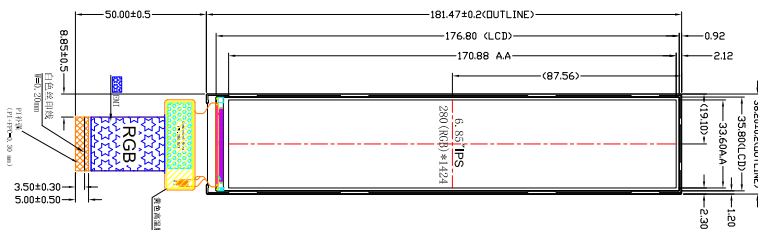
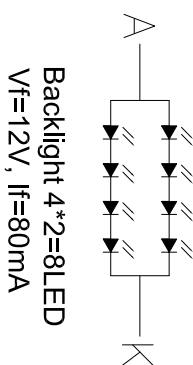
2. Mechanical Specifications


No.	Item	Specification
1	LCD Type	6.85 inch
2	Resolution	280(RGB)X1424
3	Display mode	Normally Black
4	Outline size	38.20 (H)X181.47(V)X3.45(T)mm
5	Active area	33.60(H)X170.88 (V) mm
5	Pixel pitch	40(H) X RGB X 120(V) um
6	Viewing direction	ALL
7	Display Color	16.7M
8	Surface Treatment	AG
9	Interface	RGB
10	Brightness	650 cd/m ² (typ)
11	Driver IC	NV3052

3. External Dimensions

PIN	SYMBOL
1	LEDA
2	LEDB
3	VCC (3.3V)
4	GND
5	GND
6	DEN
7	VSYNC
8	HSYNC
9	CLK
10	B7
11	B6
12	B5
13	B4
14	B3
15	B2
16	B1
17	B0
18	G7
19	G6
20	G5
21	G4
22	G3
23	G2
24	G1
25	G0
26	R7
27	R6
28	R5
29	R4
30	R3
31	R2
32	R1
33	R0
34	RESET
35	CS
36	SCL
37	SDA
38	GND
39	VCC (3.3V)
40	GND

- Notes:
1. DISPLAY TYPE: 6.85", TFT LCD
 2. DISPLAY MODE: Transmissive, Normally Black
 3. VIEWING DIRECTION: 80/80/80/80 (TYP)
 4. DRIVER IC: NV3052C
 5. BACK LIGHT: 8 chip white LEDs
 6. Lumiance 650 cd/m²(typ).
 7. OPERATING TEMP: -20° C T0 +70° C;
STORAGE TEMP: -30° C T0 +80° C;
 8. 带*编号为重点尺寸, 未注公差为±0.20;
 9. 所有材料需符合ROSH要求



TITLE: OUTLINE DIMENSION			
DRAWN BY:		D/V: AM-2801424-068E-RGB	 于都上晴电子有限公司 YU DU AMSON ELECTRONICS CO., LTD.
CHECKED BY:		REV: V0	
APPROVED BY:		SCALE: 1 : 1	UNIT: mm
SHEET NO. 1		OP 1	

SW.	DESCRIPTION OF REVISION	REASON	REVISED BY	DATE
Δ	first issue	A	XG, SU	2024/09/13

4. Interface Description

Pin No.	Symbol	Description	Remark
1	LEDA	LED anode	
2	LEDK	LED cathode	
3	VCC	Power for Digital Circuit(3.3V)	
4	GND	Ground	
5	GND	Ground	
6	DEN	Data enable pin for RGB interface operation	
7	VSYNC	Vertical synchronizing input signal	
8	HSYNC	Horizontal synchronizing input signal	
9	CLK	Dot clock signal for RGB interface operation	
10	B7	Data bus	
11	B6	Data bus	
12	B5	Data bus	
13	B4	Data bus	
14	B3	Data bus	
15	B2	Data bus	
16	B1	Data bus	
17	B0	Data bus	
18	G7	Data bus	
19	G6	Data bus	
20	G5	Data bus	
21	G4	Data bus	
22	G3	Data bus	
23	G2	Data bus	
24	G1	Data bus	
25	G0	Data bus	
26	R7	Data bus	
27	R6	Data bus	
28	R5	Data bus	
29	R4	Data bus	
30	R3	Data bus	
31	R2	Data bus	
32	R1	Data bus	
33	R0	Data bus	
34	RESET	Global reset pin.	
35	CS	Chip select signal for SPI interface operation	
36	SCL	Serial interface Clock Input	
37	SDA	Serial interface DATA Input /output	
38	GND	Ground	
39	VCC	Power for Digital Circuit(3.3V)	
40	GND	Ground	

5. Operation Specifications

5.1 Absolute Max. Rating

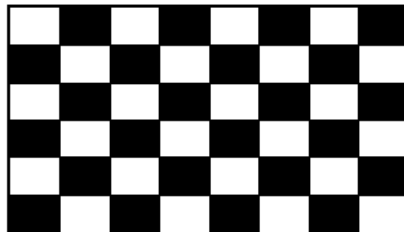
Item	Symbol	Values		Unit
		Min.	Max.	
Power Voltage	VCC	-0.3	3.6	V
Input Signal Voltage	V _I	-0.3	VCC	V
Operation Temperature	T _{OP}	-20	70	°C
Storage Temperature	T _{ST}	-30	80	°C

5.2 Typical Operation Conditions

Item	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	3.0	3.3	3.6	V
Current Consumption	I _{VCC}	-	-	-	mA
Power Consumption	P _{VCC}	-	-	-	W
Power Consumption	P _{LED}	-	0.96	-	W

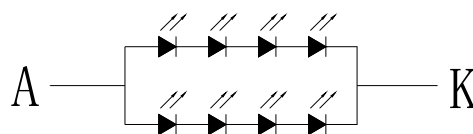
Note :1. The measuring position is the connector of LCM and the test conditions are under 25°C, Frame Rate=60Hz

2. The specified current and power consumption are under the VDD = 3.3V , 25°C, Frame Rate=60Hz condition and Mosaic pattern, The LED driving condition is I_{LED}=80mA.



5.3 LED Back Light Specification

Item	Symbol	Condition	Min	Typ.	Max	Unit
Forward Voltage	V _f	I _f =80mA	-	12	-	V
Luminance for LCM	Y _u	I _f =80mA	-	650	-	cd/m ²



Backlight 4*2=8LED
V_f=12V, I_f=80mA

5.4 Power On/Off Sequence

To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

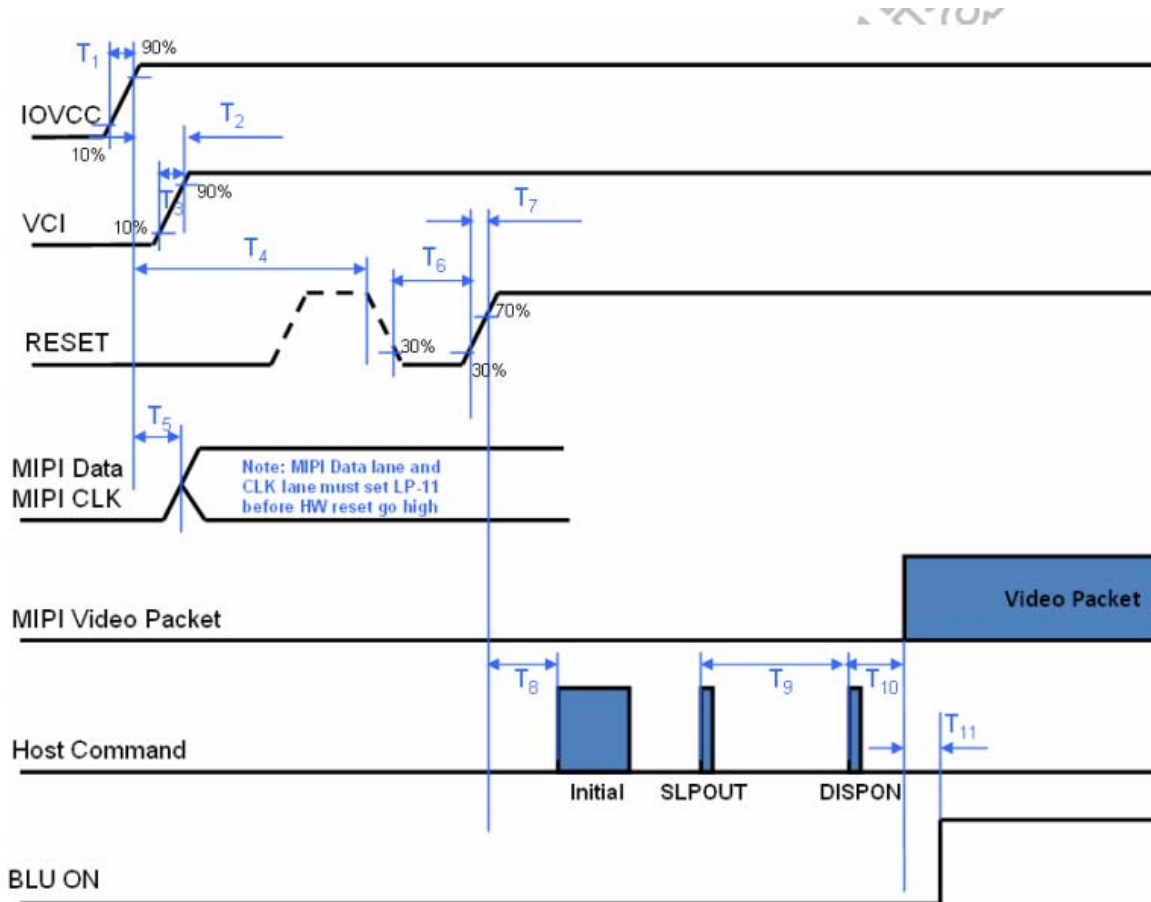


Figure 8-6: DSI Power On Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2	No Limit			ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7	No Limit			ns
T8	15	-	-	ms
T9	120	-	-	ms
T10	No Limit			ms
T11	100	150	-	ms

Table 8-1: DSI Power On Timing of Power IC Mode

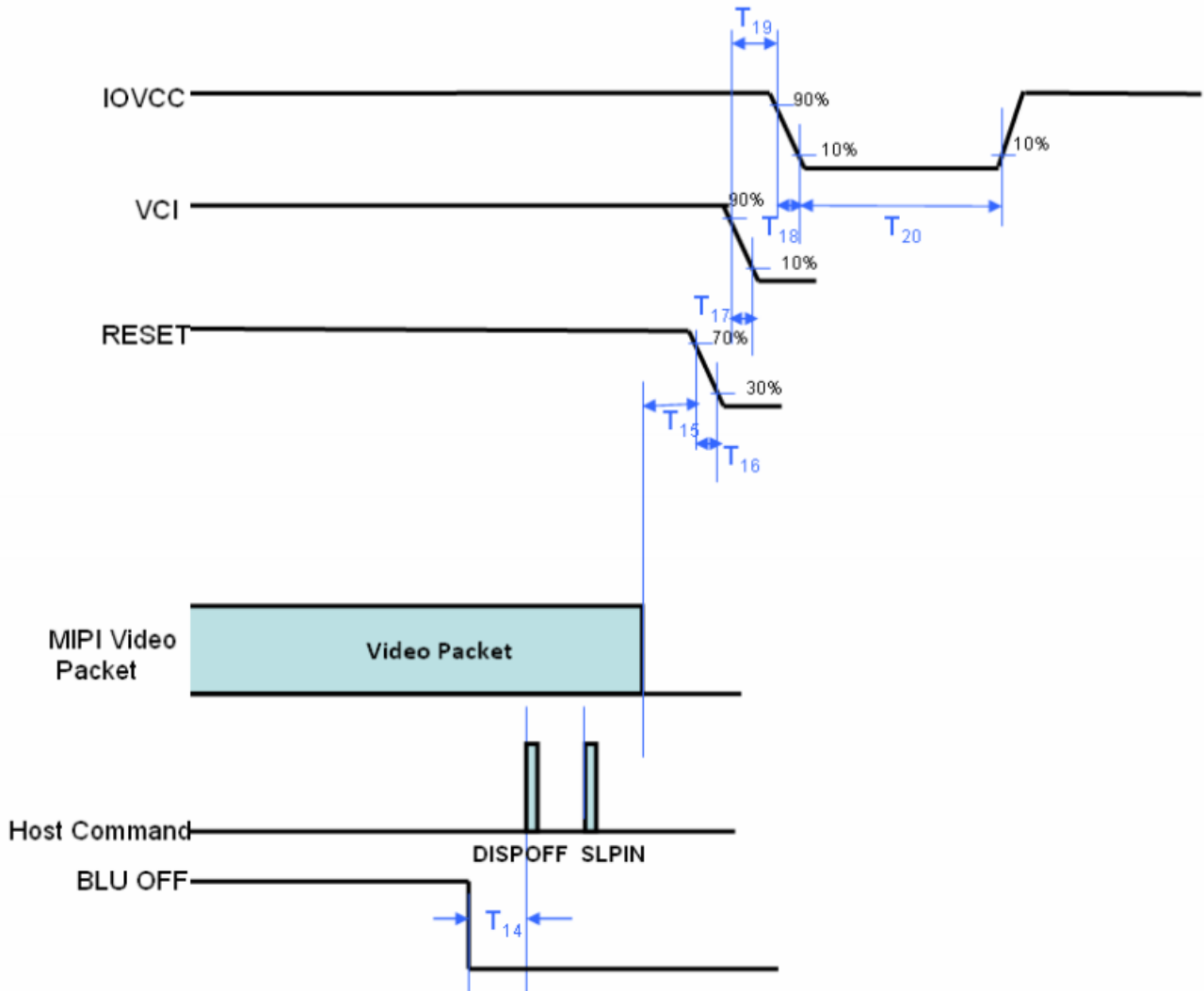


Figure 8-7: DSI Power Off Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	No Limit			ms
T19	No Limit			ms
T20	500			ms

Table 8-2: DSI Power Off Timing of Power IC Mode

6. Signal Timing Characteristics

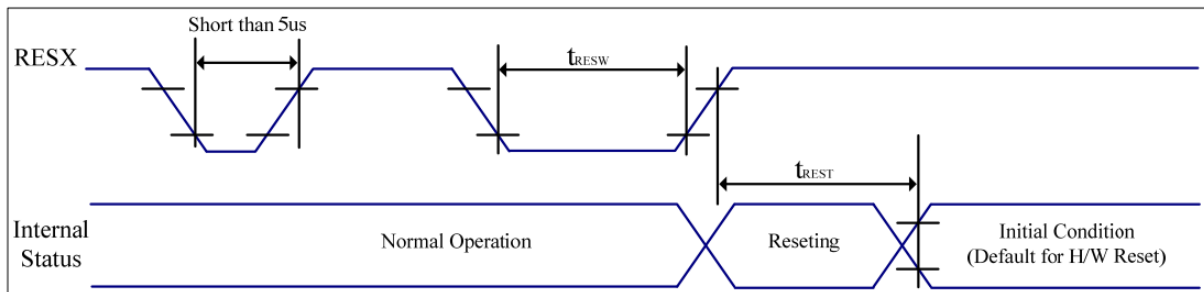
6.1 DC electrical Characteristics

(VCI=2.5V~6.0V, IOVCC=1.65V~3.6V, Ta=-30°C~70°C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.5	2.8	6.0	V	
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V	
MIPI interface operating voltage	VDDAM	MIPI supply voltage	1.75	-	6.0	V	Note1
Input/Output							
Logic High level input voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3*IOVCC	V	
Logic High level output voltage	VOH	IOH = -0.1mA	0.8*IOVCC	-	IOVCC	V	
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2*IOVCC	V	
Logic Input leakage current	IIL	Vin=IOVCC or VSS	-0.1	-	+0.1	uA	

6.2 AC electrical Characteristics

6.2.1 Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V, Ta = -30°C to 70°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

Note 1: Due to an electrostatic discharge on RESX line, spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode), then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (T_{rest}) which lasted 5ms. The loading operation will be done every time during this reset.

6.2.2 Serial interface characteristics (SPI)

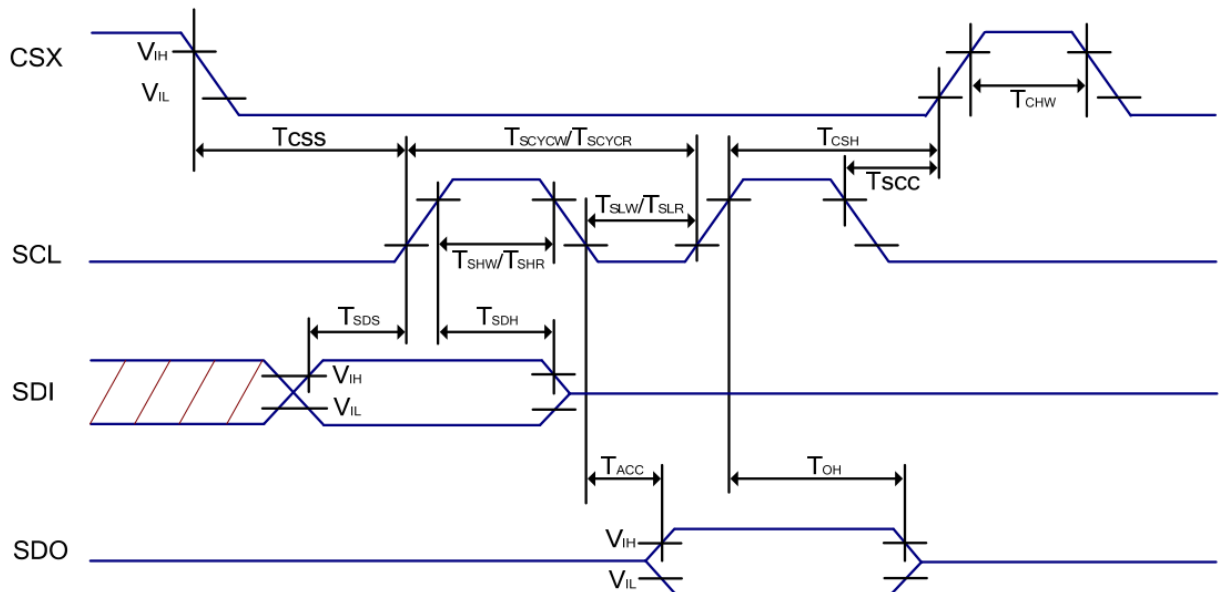


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MI N	MA X	Unit	Description
CSX	T _{CS}	Chip select setup time	15	-	ns	-
	T _{CSH}	Chip select hold time	15	-	ns	
	T _{SCC}	Chip select setup time	20	-	ns	
	T _{CHW}	Chip “H” pulse width	40	-	ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	66	-	ns	-
	T _{SHW}	SCL “H” pulse width (Write)	10	-	ns	
	T _{SLW}	SCL “L” pulse width (Write)	10	-	ns	
	T _{SCYCR}	Serial clock cycle (Read)	150	-	ns	-
	T _{SHR}	SCL “H” pulse width (Read)	60	-	ns	
	T _{SLR}	SCL “L” pulse width (Read)	60	-	ns	
SDI	T _{SDS}	Data setup time	10	-	ns	-
	T _{SDH}	Data hold time	10	-	ns	
	T _{ACC}	Access time	10	50	ns	For maximum C _L =30pF For minimum C _L =8pF
	T _{OH}	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V, Ta=-30 to 70°C

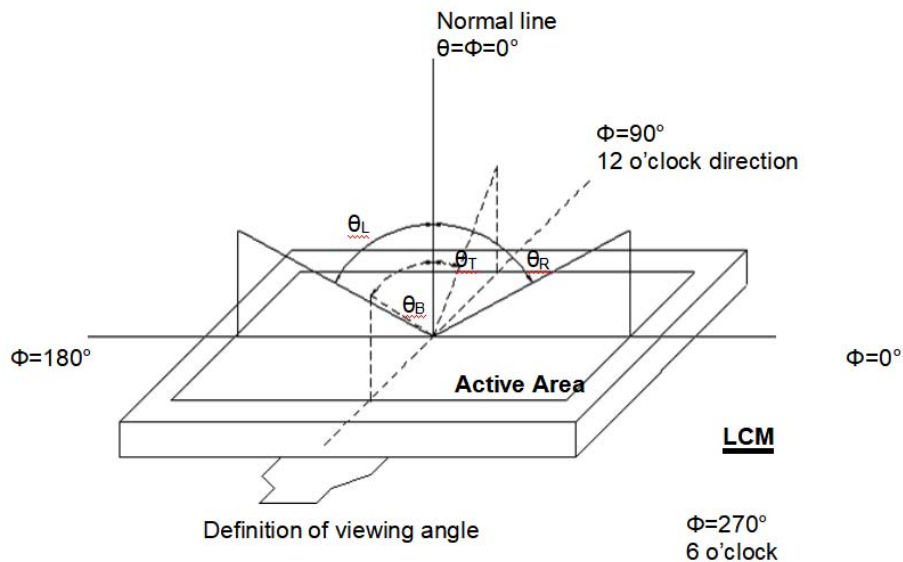
Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7. Optical specifications

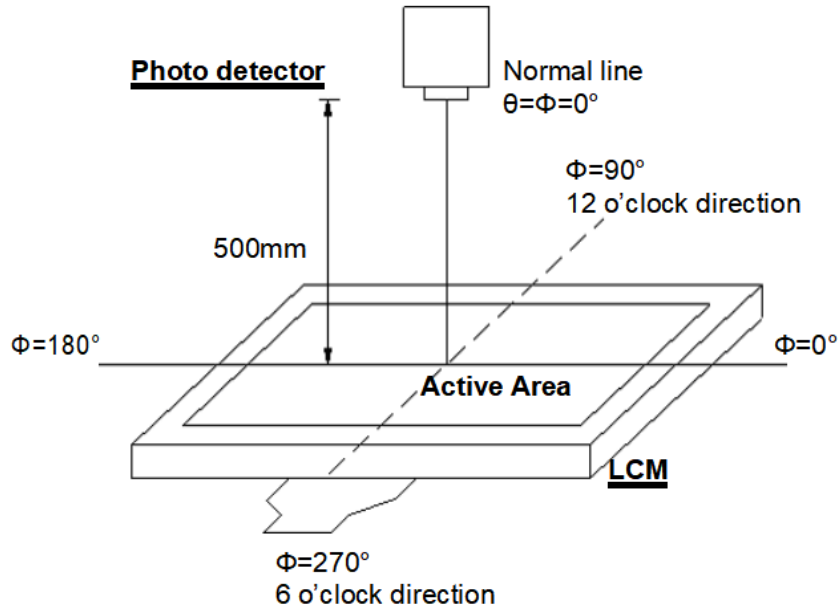
Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR \geq 10)	θ_L	$\Phi=180^\circ$ (9 o'clock)	-	85	-	degree	Note 1
	θ_R	$\Phi=0^\circ$ (3 o'clock)	-	85	-		
	θ_T	$\Phi=90^\circ$ (12 o'clock)	-	85	-		
	θ_B	$\Phi=270^\circ$ (6 o'clock)	-	85	-		
Response time Rise + Fall	T_{RT}	Normal $\theta=\Phi=0^\circ$	-	-	35	msec	Note 3
Contrast ratio	CR		-	900	-	-	Note 4
Color chromaticity	W_X		-	0.301	-	-	Note 2 Note 5 Note 6
	W_Y		-	0.329	-	-	
NTSC	Ratio		-	65	-	%	
Luminance	L		-	650	-	cd/m ²	Note 6

Note 1: Definition of viewing angle range



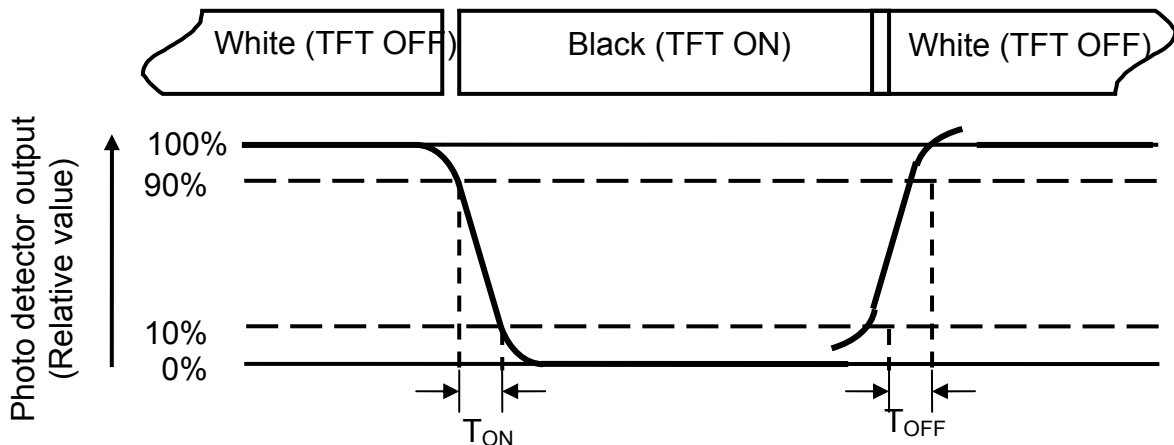
Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height: 1.2mm, Response time is measured by Photo detector TOPCON BM-7A, other items are measured by BM-7A/Field of view: 1° /Height: 500mm.)



Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel.

8. Reliability Test Conditions And Methods

Item	Test Conditions	Remark
High Temperature Storage	Ta = 80°C 96 hrs	
Low Temperature Storage	Ta = -30°C 96 hrs	
High Temperature Operation	Ts = 70°C 96 hrs	
Low Temperature Operation	Ta = -20°C 96 hrs	
Operate at High Temperature and Humidity	50°C, 90%RH max. 96 hrs	Operation
Thermal Shock	-20°C~+60°C 10cycles 1 Hrs/cycle	Non-operation
Electrostatic Discharge	Contact=±4KV, class B Air=±8KV, class B	

Note1: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

Note2: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

9. Package Drawing

TBD