Specification for Approval

Customer:_____

Model Name:_____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

RECORD OF REVISION

REV NO.	REV DATE	CONTENTS	Note
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Contents

1.0 General Description

1.1 Application

- 绘图板

1.2 General Specification

1.2.1.General FOB Specification(Table 1.)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	293.76 (H) x 165.24 (V)	mm	
Number of pixels	1920 (H) x 1080 (V)	pixels	
Pixel pitch	0.153 (H) x 0.153 (V)	mm	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M	colors	
Display mode	Normally Black		
Dimensional outline	305.2(H)*187.9(V) *2.6(D)	mm	
Weight	-	g	
Back-light	Lower Down side, 1-LED Lighting Bar type		Note 1
Power consumption	-	W	
	-	W	
	-	W	

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings> Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	LCD_VCC	-0.3	5	V	Note 1
BLU Power Supply Voltage	BL_PWR	-0.3	27	V	
Operating Temperature	T_{OP}	0	+50	℃	Note 2
Storage Temperature	T_{ST}	-20	+60	℃	

Notes : 1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.
90 % RH Max. (40 ^{O}C ≥ Ta)
Maximum wet - bulb temperature at 39 ^{O}C or less. (Ta > 40 ^{O}C) No condensation.

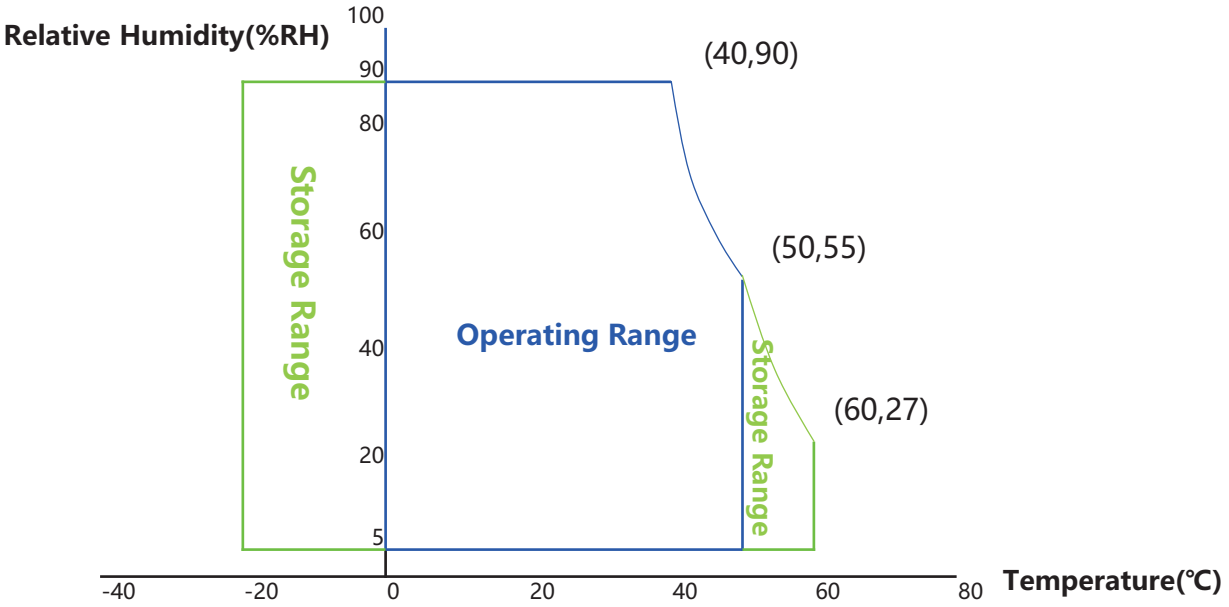


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical specifications > Ta=25+/-2°C

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
Power Supply Input Voltage	LCD_VCC	3.0	3.3	3.6	V	Note 1
Power Supply Current	I_{LCD_VCC}	-	-	-	mA	
In-Rush Current	I_{RUSH}	-	-	-	A	
Permissible Input Ripple Voltage	V_{RF}	-	-	-	mV	

Notes : 1. The supply voltage is measured and specified at the interface connector of FOB.
The current draw and power consumption specified is for 3.3V at 25 ℃

Ta=25+/-2°C

3.2 Back-light Unit

< Table 3.2 LED Driving guideline specifications >

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power supply voltage for LED Driver		BL_PWR	5	12	21	V	
Power supply Current for Back light		V_{BLU}	-	21	-	V	
Power supply Current for Back light		I_{BLU}	-	160	-	mA	背光灯串：8并7串
Power supply for Back light		P_{BL_PWR}	-	3.95	-	W	LED Power Consumption follow customerrequirements
EN Control Level	Backlight on	V_{ENH}	1.6	-	BL_PWR	V	EN logic high voltage
	Backlight off	V_{ENL}	0	-	0.8	V	EN logic low voltage
PWM Control Level	PWM High Level	V_{PML}	1.6	-	BL_PWR	V	
	PWM Low Level	V_{PML}	0	-	0.8	V	
PWM Control Frequency		F_{PWM}	0.2	-	20	KHz	
Duty Ratio		-	25	-	100	%	

Notes : 1. Calculator Value for reference $I_{BLU} \times V_{BLU} = P_{BL\_PWR}$*85%

2. The LED Life-time define as the estimated time to 50% degradation of initial luminous under the condition of the ambient temperature of 25℃.

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	85	-	Deg.	Note 1
		Θ_9		-	85	-	Deg.	
	Vertical	Θ_{12}		-	85	-	Deg.	
		Θ_6		-	85	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	800	1000	-	-	
Luminance of White	5 Points	Y_w	Θ = 0° I_{LED} = 23.5mA	250	-	-	cd/m^2	
White Luminance uniformity	5 Points	ΔY5		80	-	-	-	Type.
	9 Points	ΔY9		75	-	-	-	
White Chromaticity		x_w	Θ = 0°	0.283	0.313	0.343	-	
		y_w		0.293	0.329	0.359	-	
Reproduction of color	Red	x_R	Θ = 0°	-0.03	0.653	+0.03	-	
		y_R			0.341		-	
	Green	x_G			0.322		-	
		y_G			0.618		-	
	Blue	x_B			0.149		-	
		y_B			0.066		-	
Gamut		-	-	68	72	-	%	
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	30	35	Ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	-	%	

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state .
(see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.
(see FIGURE 2 and FIGURE 3).

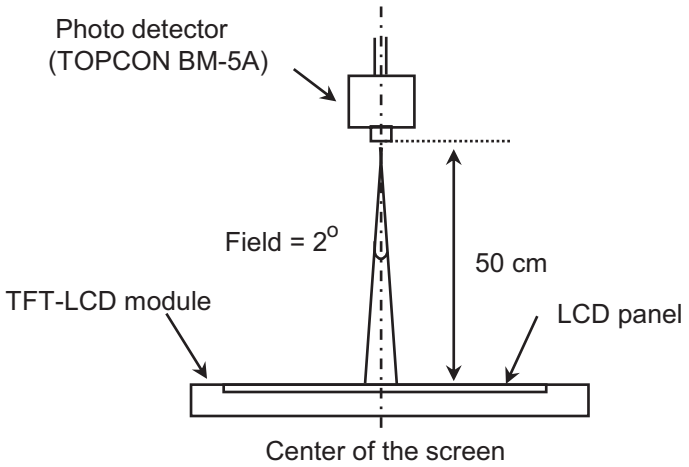
5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as FIGURE 4 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.
(See FIGURE 5).

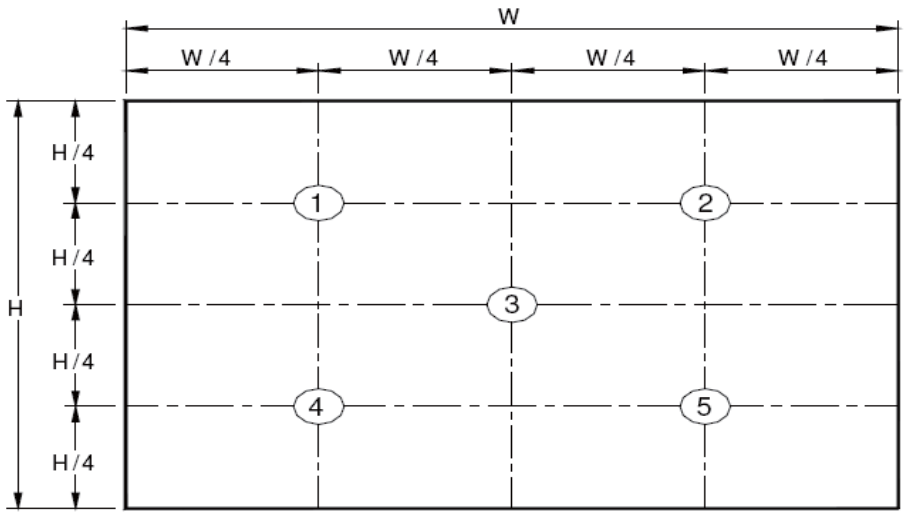
4.3 Optical measurements

Figure 1. Measurement Set Up



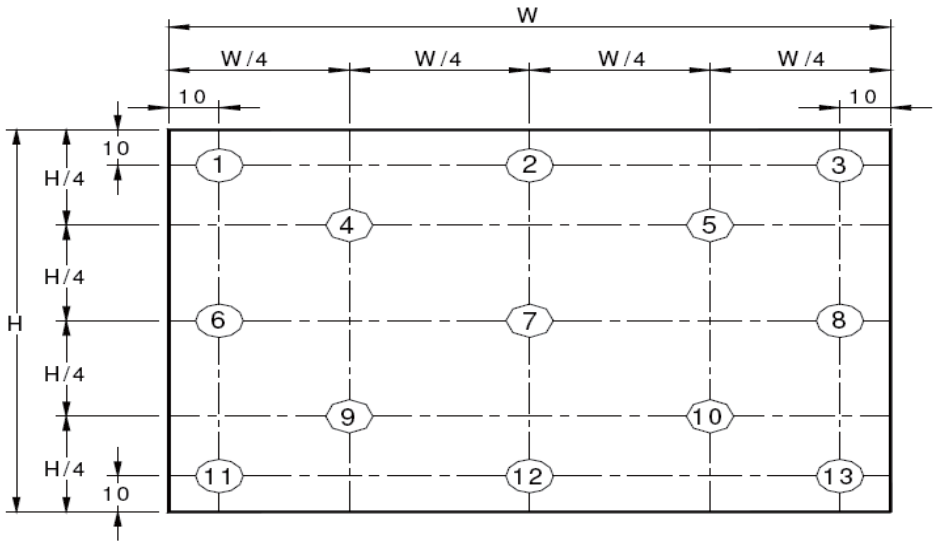
Optical characteristics measurement setup

Figure 2. White Luminance and Uniformity Measurement Locations (5 points)



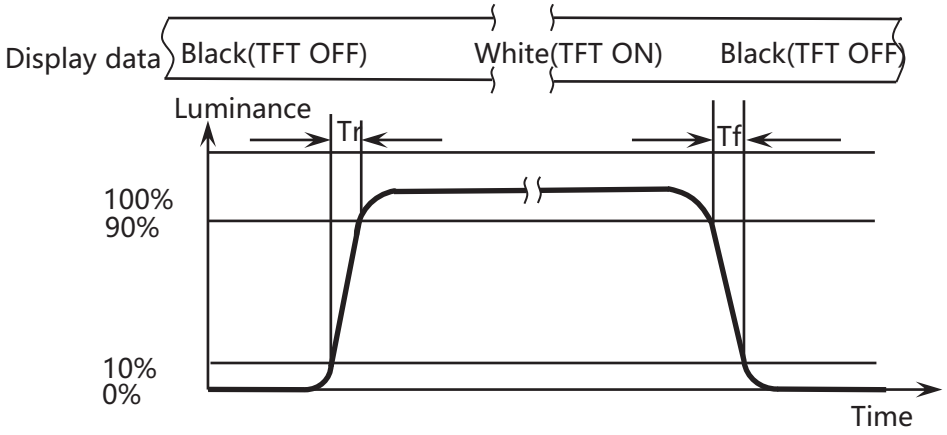
Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

Figure 3. Uniformity Measurement Locations (13 points)



The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see FIGURE 2) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see FIGURE 3).

Figure 4. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 4 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr and 90% to 10% is Tf.

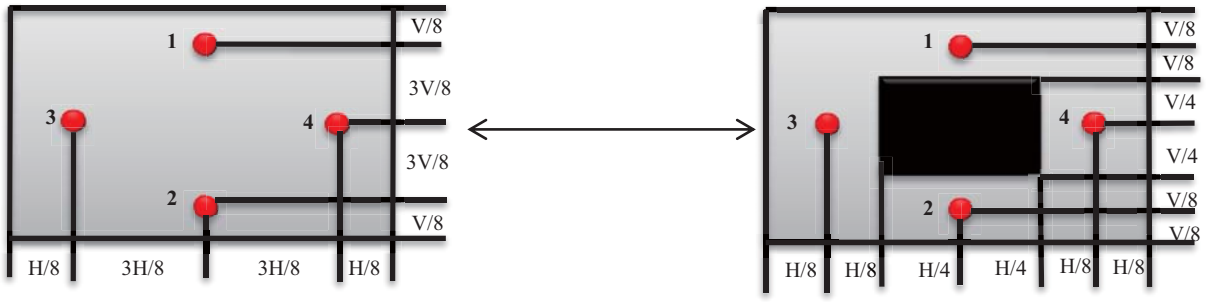


Figure 5. Cross Talk Modulation Test Description

$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 5)

The test system: PR730

5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

The electronics interface connector is MSAK24025P30.
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

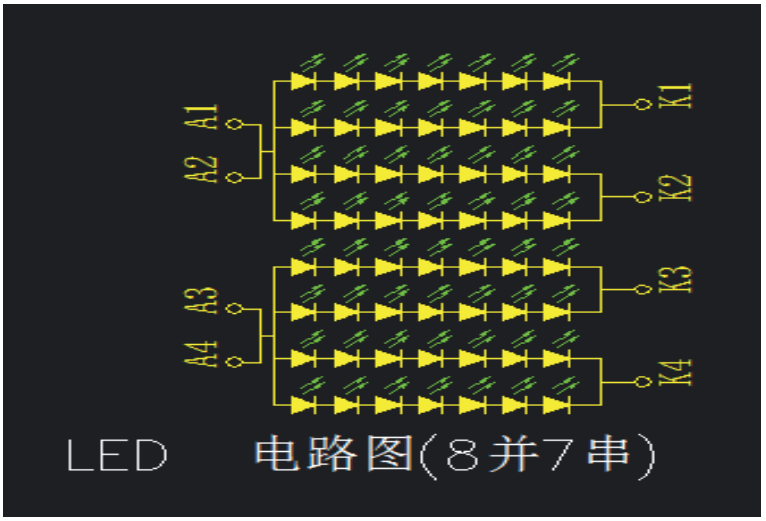
Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	NC	Non Connection
2	H-GND	Ground
3	LAN1_N	Complement Signal Link_Lane1
4	LAN1_P	True Signal Link_Lane1
5	H-GND	Ground
6	LAN0_N	Complement Signal Link_Lane0
7	LAN0_P	True Signal Link_Lane0
8	H-GND	Ground
9	AUXP	True Signal Link_Auxiliry Channel
10	AUXN	Complement Signal Link_Auxiliry Channel
11	H-GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel self test enable
15	H-GND	Ground
16	H-GND	Ground
17	HPD	HPD(Hot Plug Detect) Signal Pin
18	BL_GND	High Speed Ground
19	BL_GND	High Speed Ground
20	BL_GND	High Speed Ground
21	BL_GND	High Speed Ground
22	BL_EN	Backlight on/off Control pin
23	BL_PWM	Back light PWM Dimming
24	NC	Non Connection
25	NC	Non Connection
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	Non Connection

5.2 Back-light & LED Interface Connection

The electronics interface connector is 20599-015E-01

<Table 7. Pin Assignments for the BLU & FOB Connector>

Pin No.	Symbol
1	A1
2	A2
3	A3
4	A4
5	NC
6	NC
7	NC
8	K1
9	K1
10	K2
11	K2
12	K3
13	K3
14	K4
15	K4



6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV133FHM-N41 is operated by the DE only.

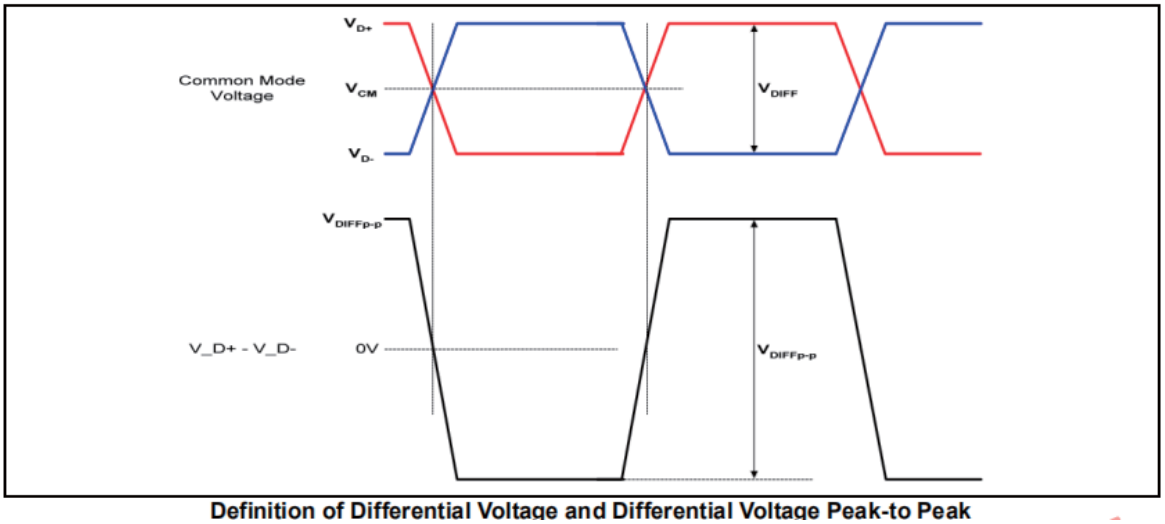
Item		Symbols	Min	Typ	Max	Unit
PClock	Frequency	1/Tc	-	147.8	-	MHz
Frame Period		Tv	-	1120	-	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	-	2200	-	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 8.

<Table 9. eDP Rx Interface Timing Specification>

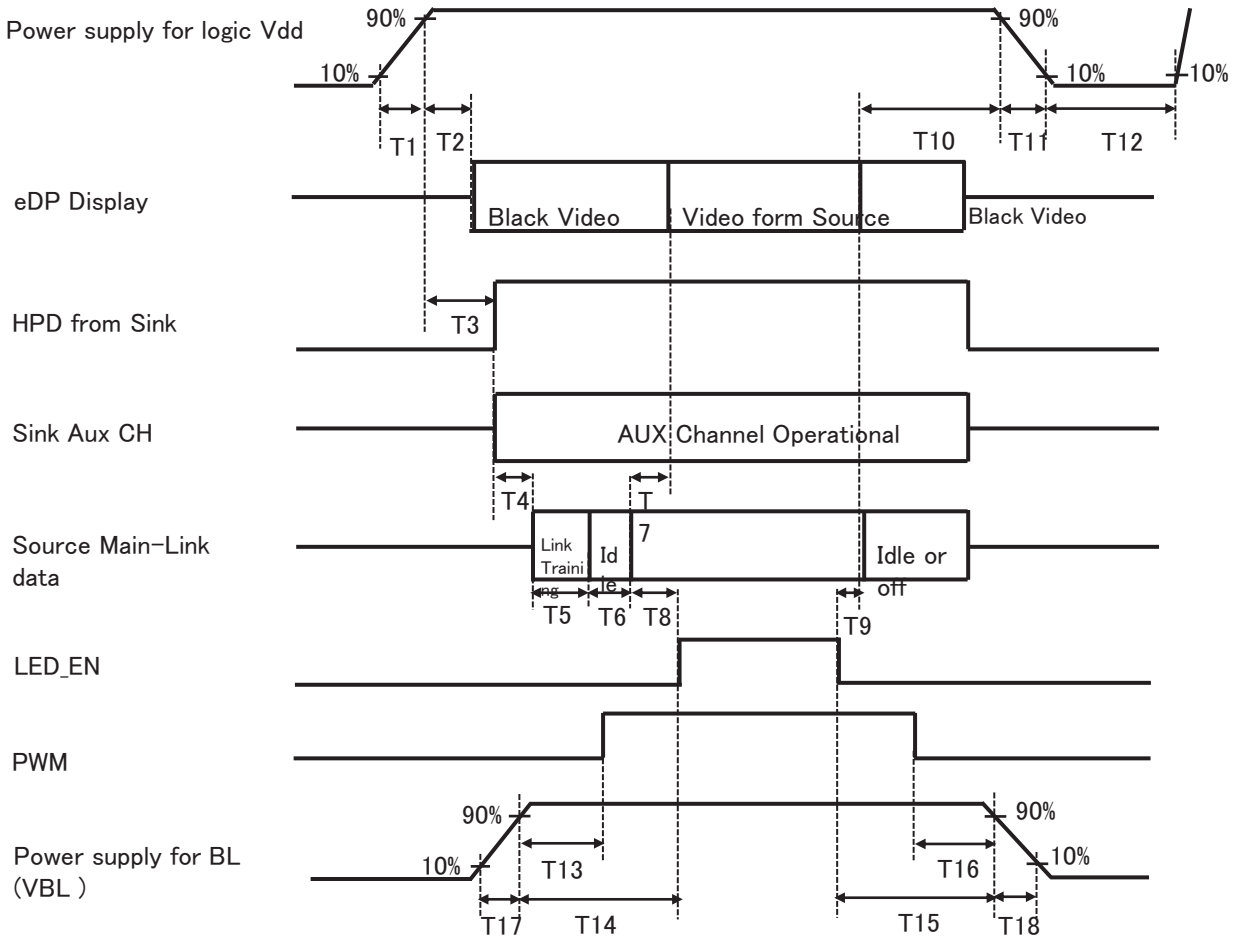
Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock	ssc	0	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	120	-	1200	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2.0	V	
Differential termination resistance	$R_{RX-DIFF}$	-	100	-	Ω	
Single-ended termination resistance	R_{RX-SE}	-	-	-	Ω	
Rx short circuit current limit	I_{RX_SHORT}	0	-	50	mA	



Definition of Differential Voltage and Differential Voltage Peak-to Peak

7.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off seq uence shall be as shown in below



- 0.5ms ≤ T1 ≤ 10 ms
- 0ms ≤ T2 ≤ 200 ms
- 0ms ≤ T3 ≤ 200 ms
- 10ms ≤ T13
- 20ms ≤ T14
- 0.5ms ≤ T17 ≤ 20ms
- 0ms ≤ T7 ≤ 50ms
- 0ms ≤ T10 ≤ 500 ms
- 3ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 20ms ≤ T15
- 10ms ≤ T16
- 0.5ms ≤ T18 ≤ 20ms

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or k eep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

8.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 10. Reliability test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60˚C , 60%RH, 96 hrs	
2	Low temperature storage test	Ta = -20˚C , 96 hrs	
3	High temperature & high humidity operation test	Ta = 50˚C , 80%RH, 96 hrs	
4	High temperature operation test	Ta = 50˚C , 60%RH, 96 hrs	
5	Low temperature operation test	Ta = 0˚C , 240 hrs	
6	Thermal shock	Ta = -20 ˚C ↔ 60 ˚C (0.5 hr), 60%±3%RH, 10 cycle	
7	Vibration test(non-operating)	Ta = 25˚C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour	Note 1
8	Shock test(non-operating)	Ta = 25˚C , 60%RH, 220G, Half Sine Wave 2msec ± X, ± Y, ± Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ±8 KV Contact : 150 pF, 330Ω, ±4 KV Ta = 25˚C , 60%RH,	Note 2

Note1:Ts is the temperature of panel's surface.
Note2: Ta is the ambient temperature of sample.
Note3: Before cosmetic and function test, the product must have enough recovery timeat least 2 hours at room temperature.
Note 4: in the standard condition, there shall be no practical problem that may aftect thedisplay function. After the reliability test, the product only guarantees operation, but don'guarantee all of the cosmetic specification.

9.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

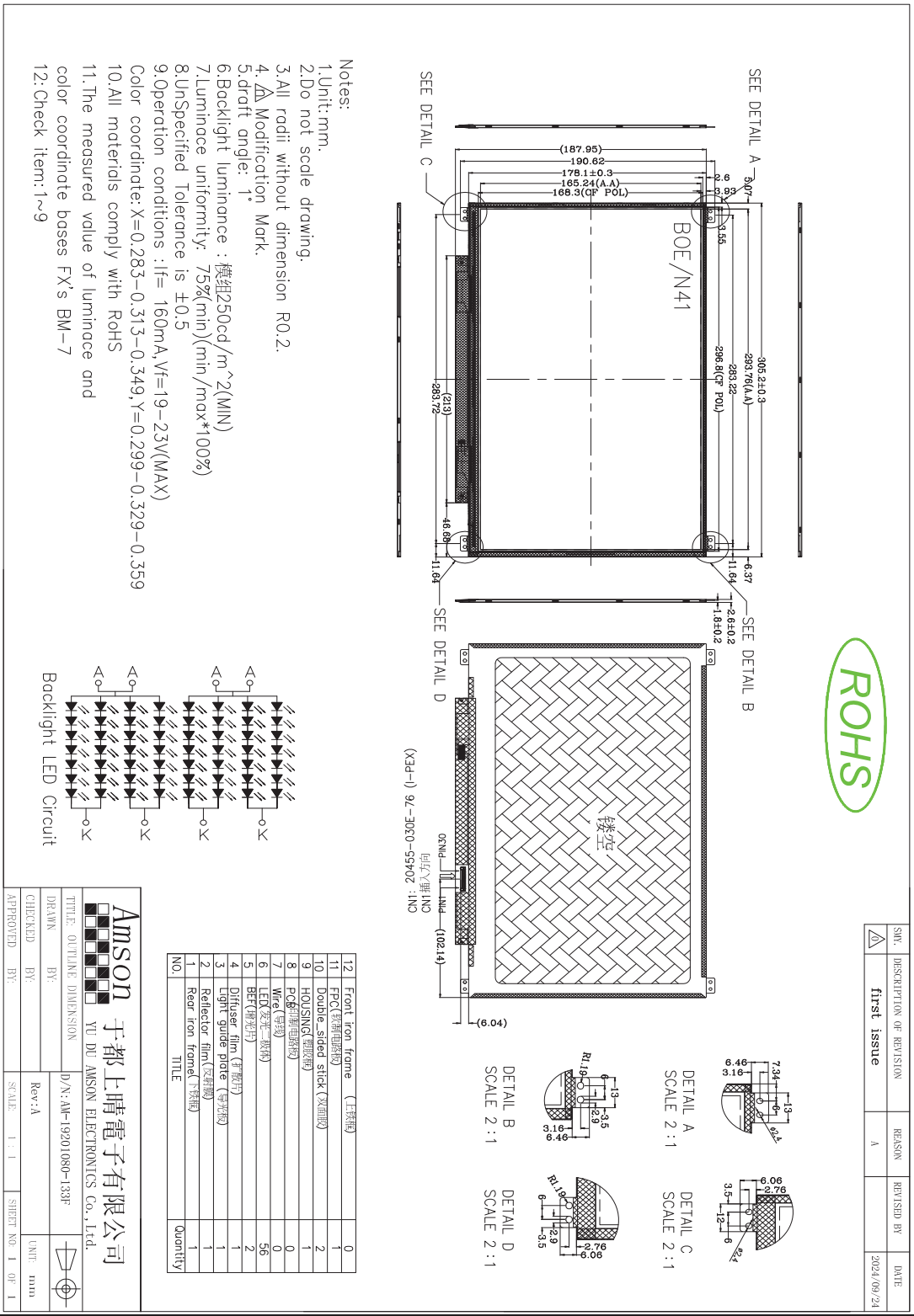
(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

10. Total Solution Outline Dimension



NO.	Quantity
12	Front iron frame (上铁框) 1
11	FPC(软排电路板) 1
10	Double_sided stick(双面胶) 2
9	HOUSING(塑胶框) 1
8	PCB(印刷电路板) 1
7	Wire(导线) 0
6	LED(发光二极体) 56
5	BEF(增光片) 2
4	Diffuser film (扩散片) 1
3	Light guide plate (导光板) 1
2	Reflector film(反射膜) 1
1	Rear iron frame(下铁框) 1
TITLE	

11 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	1F	31		3108	ID = 3108
0B		08	8			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	21	33		25	
11	Year of Manufacture	1C	28		2022	Manufactured in 2022
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	95	149		-	Refer to right table
15	Max H image size	1D	29		29	29.376 cm (Approx)
16	Max V image size	11	17		17	16.524 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	E7	231		-	Red / Green Low Bits
1A	Blue/White low bits	B0	176		-	Blue / White Low Bits
1B	Red x high bits	95	149	604	0.651	Red (x) = 10010101 (0.651)
1C	Red y high bits	5C	92	358	0.345	Red (y) = 01011100 (0.345)
1D	Green x high bits	59	89	338	0.331	Green (x) = 01011001 (0.331)
1E	Green y high bits	94	148	568	0.612	Green (y) = 10010100 (0.612)
1F	Blue x high bits	29	41	157	0.151	Blue (x) = 00101001 (0.151)
20	BLue y high bits	22	34	122	0.057	Blue (y) = 00100010 (0.057)
21	White x high bits	50	80	321	0.303	White (x) = 01010000 (0.303)
22	White y high bits	54	84	337	0.325	White (y) = 01010100 (0.325)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	C1	193		147.8	147.8MHz Main clock
37		37	55			
38		80	128		1920	Hor Active = 1920
39		CC	204		280	Hor Blanking = 280
3A		71	113		–	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		38	56		1080	Ver Active = 1080
3C		28	40		40	Ver Blanking = 40
3D		40	64		–	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		36	54		3	V sync Offset = 3 line
41		00	0		6	V Sync Pulse width : 6 line
42		26	38		294	Horizontal Image Size = 294 mm (Low 8 bits)
43		A5	165		165	Vertical Image Size = 165 mm (Low 8 bits)
44		10	16		–	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		–	Refer to right table

Detailed timing/monitor descriptor #2	2B	43		147.8	147.8MHz Main clock
	39	57			
	80	128		1920	Hor Active = 1920
	18	24		280	Hor Blanking = 280
	71	113		–	4 bits of Hor. Active + 4 bits of Hor. Blanking
	38	56		1080	Ver Active = 1080
	28	40		40	Ver Blanking = 40
	40	64		–	4 bits of Ver. Active + 4 bits of Ver. Blanking
	30	48		48	Hor Sync Offset = 48
	20	32		32	H Sync Pulse Width = 32
	36	54		3	V sync Offset = 3 line
	00	0		6	V Sync Pulse width : 6 line
	26	38		294	Horizontal Image Size = 294 mm (Low 8 bits)
	A5	165		165	Vertical Image Size = 165 mm (Low 8 bits)
	10	16		–	4 bits of Hor Image Size + 4 bits of Ver Image Size
	00	0		0	Hor Border (pixels)
	00	0		0	Vertical Border (Lines)
	1A	26		–	Refer to right above table
Detailed timing/monitor descriptor #3	00	0			Nvidia nvDPS (Refer the tab of nvDPS) Lowest refresh rate that does not cause any visual/optical side effect
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			
	00	0			

Detailed timing/monitor descriptor #4	00	0			Detailed Timing Description #4
	00	0			Flag
	00	0			Reserved
	02	2			For Brightness Table and Power consumption
	00	0			Flag
	0D	13		-	PWM % [7:0] @ Step 0
	49	73		-	PWM % [7:0] @ Step 5
	FF	255		-	PWM % [7:0] @ step 10
	0A	10		-	Nits [7:0] @ Step 0
	3C	60		-	Nits [7:0] @ Step 5
	6E	110		-	Nits [7:0] @ Step 10
	16	22		-	Panel Electronics Power @32x32 Chess Pattern = 800mW
	12	18		-	Backlight Power @60 nits = 837.433155080214mW
	20	32		-	Backlight Power @Step 10 = 2900mW
	6E	110		-	Nits @ 100% PWM Duty = 220nit
	00	0			Format : terminate with ASCII code 0Ah and pad field with ASCII code 20h
	00	0			
	00	0			
Extension flag	00	0		1	0 ：1個EDID；N-1：N个EDID
Checksum	E4	228	228	-	