Version: A

2024-06-13

# Specification for Approval

Customer:	
Model Name:	

Si	Customer approval		
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

Version: A

2024-06-13

# **Revision Record**

REV NO.	REV DATE	CONTENTS	Note
Α	2024-06-13	NEW ISSUE	
<u> </u>	<u> </u>		ļ

Version: A

2024-06-13

# **Table of Contents**

List	Description	Page No.
	Cover	1
	Revision Record	2
	Table of Contents	3
1	Scope	4
2	General Information	4
3	External Dimensions	5
4	Interface Description	6
5	Absolute Maximum Ratings	7
6	DC Characteristics	7
7	Timing Characteristics	8
8	Backlight Characteristics	15
9	Optical Characteristics	16
10	Reliability Test Conditions and Methods	18
11	Inspection Standard	19
12	Handling Precautions	24
13	Precaution for Use	25
14	Packing Method	25



Version: A

2024-06-13

### 1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.

If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

### 2. General Information

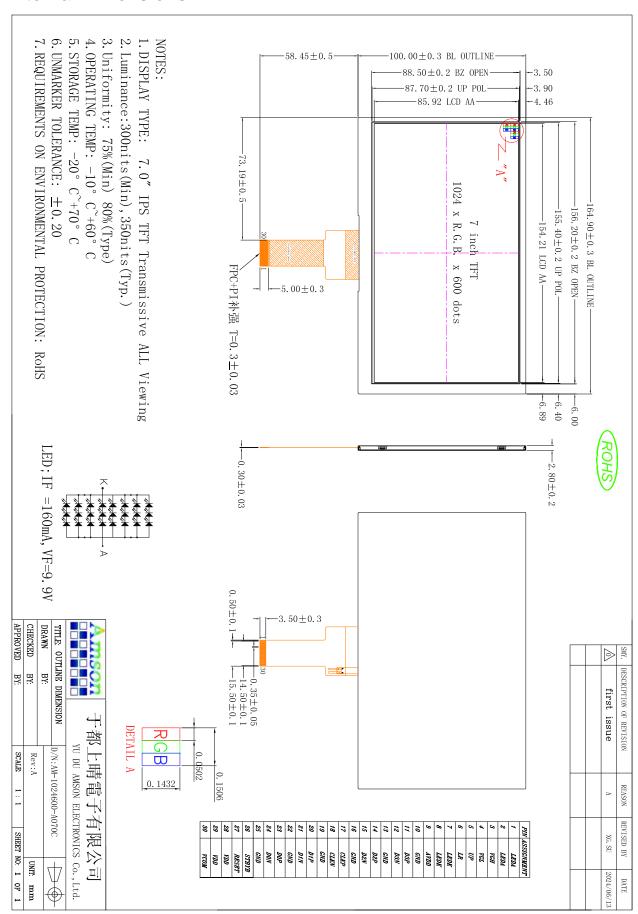
TITEM	STANDARD VALUES	UNITS
LCD type	7.0"TFT	
Dot arrangement	1024(RGB)×600	dots
Color filter array	RGB vertical stripe	
Display mode	Normally Black , Transmissive	-
Gray Scale Inversion Direction	ALL	
Eyes Viewing Direction	85/85/85	
LCM size	165(W)×100.0(H)×2.8(T)	mm
Active area	154.21(W)×85.92(H)	mm
Dot pitch	0.1506(W)×0.1432(H)	mm
Interface	MIPI	
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
LCM Driver IC	EK79007AD/EK73217BCGA	
Back Light	24White LED	



Version: A

2024-06-13

#### 3. External Dimensions





Version: A

2024-06-13

## 4. Interface Description

## **TFT**

High-Z.	I F I	DIM MARKE	DECORPTION
LED backlight (Anode).  LED backlight (Anode).  VGH Positive Power for TFT.  VGL Negative Power for TFT.  UP Jp / Down Display Control.  LED Left or Right Display Control.  LED backlight (Cathode).  LED backlight (Cathode).  LED backlight (Cathode).  LED backlight (Cathode).  MIPI differential data lane 3 input (Positive).  MIPI differential data lane 3 input (Negative) .  MIPI differential data lane 2 input (Negative) .  MIPI differential data lane 2 input (Negative) .  MIPI differential clock input (Positive).  MIPI differential clock input (Negative) .  CLKP MIPI differential clock input (Negative) .  MIPI differential data lane 1 input (Negative) .  MIPI differential data lane 0 input (Negative) .  MIPI differential data lane 0 input (Negative) .  STBYB = "H" , normal operation(default) STBYB = "H" , normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.			DESCRIPTION
2 LEDA 3 VGH Positive Power for TFT. 4 VGL Negative Power for TFT. 5 UP Up / Down Display Control. 6 LR Left or Right Display Control. 7 LEDK 8 LEDK 9 AVDD Analog Power. 10 GND Power ground. 11 D3P MIPI differential data lane 3 input (Positive). 12 D3N MIPI differential data lane 3 input (Negative) . 13 GND Power ground. 14 D2P MIPI differential data lane 2 input (Positive). 15 D2N MIPI differential data lane 2 input (Negative) . 16 GND Power ground. 17 CLKP MIPI differential clock input (Positive). 18 CLKN MIPI differential clock input (Negative) . 19 GND Power ground. 20 D1P MIPI differential data lane 1 input (Positive). 21 D1N MIPI differential data lane 1 input (Negative) . 22 GND Power ground. 23 D0P MIPI differential data lane 1 input (Negative) . 24 D0N MIPI differential data lane 0 input (Negative) . 25 GND Power ground. 26 STBYB "H" normal operation(default) STBYB = "H" normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar high-Z."			LED backlight (Anode).
4 VGL Negative Power for TFT. 5 UP Up / Down Display Control. 6 LR Left or Right Display Control. 7 LEDK 8 LEDK 8 LEDK 9 AVDD Analog Power. 10 GND Power ground. 11 D3P MIPI differential data lane 3 input (Positive). 12 D3N MIPI differential data lane 3 input (Negative) . 13 GND Power ground. 14 D2P MIPI differential data lane 2 input (Positive). 15 D2N MIPI differential data lane 2 input (Negative) . 16 GND Power ground. 17 CLKP MIPI differential clock input (Positive). 18 CLKN MIPI differential clock input (Negative). 19 GND Power ground. 20 D1P MIPI differential data lane 1 input (Positive). 21 D1N MIPI differential data lane 1 input (Negative) . 22 GND Power ground. 23 D0P MIPI differential data lane 1 input (Negative) . 24 D0N MIPI differential data lane 0 input (Negative) . 25 GND Power ground. 26 STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.			3 4 (
5 UP Up / Down Display Control. 6 LR Left or Right Display Control. 7 LEDK 8 LEDK 9 AVDD Analog Power. 10 GND Power ground. 11 D3P MIPI differential data lane 3 input (Positive). 12 D3N MIPI differential data lane 3 input (Negative) . 13 GND Power ground. 14 D2P MIPI differential data lane 2 input (Positive). 15 D2N MIPI differential data lane 2 input (Negative) . 16 GND Power ground. 17 CLKP MIPI differential clock input (Positive). 18 CLKN MIPI differential clock input (Negative). 19 GND Power ground. 20 D1P MIPI differential data lane 1 input (Positive). 21 D1N MIPI differential data lane 1 input (Negative) . 22 GND Power ground. 23 D0P MIPI differential data lane 1 input (Negative) . 24 D0N MIPI differential data lane 0 input (Negative) . 25 GND Power ground. 26 STBYB = "H" , normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	3	VGH	Positive Power for TFT.
6 LR Left or Right Display Control.  7 LEDK  8 LEDK  LED backlight (Cathode).  9 AVDD Analog Power.  10 GND Power ground.  11 D3P MIPI differential data lane 3 input (Positive).  12 D3N MIPI differential data lane 3 input (Negative).  13 GND Power ground.  14 D2P MIPI differential data lane 2 input (Positive).  15 D2N MIPI differential data lane 2 input (Negative).  16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative).  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative).  25 GND Power ground.  26 STBYB "H", normal operation(default)  STBYB = "L", timing controller, source driver will turn off, all output ar	4	VGL	Negative Power for TFT.
7 LEDK 8 LEDK 9 AVDD Analog Power. 10 GND Power ground. 11 D3P MIPI differential data lane 3 input (Positive). 12 D3N MIPI differential data lane 3 input (Negative). 13 GND Power ground. 14 D2P MIPI differential data lane 2 input (Positive). 15 D2N MIPI differential data lane 2 input (Negative). 16 GND Power ground. 17 CLKP MIPI differential clock input (Positive). 18 CLKN MIPI differential clock input (Negative). 19 GND Power ground. 20 D1P MIPI differential data lane 1 input (Positive). 21 D1N MIPI differential data lane 1 input (Negative). 22 GND Power ground. 23 D0P MIPI differential data lane 1 input (Negative). 24 D0N MIPI differential data lane 0 input (Positive). 25 GND Power ground. 26 STBYB = "H" ,normal operation(default) STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar	5	UP	Up / Down Display Control.
LEDK  Beacklight (Cathode).  LED backlight (Cathode).  AVDD Analog Power.  Beach AVDD Analog Power.  Beach AVDD Analog Power.  Analog Power ground.  Beach AVDD Analog Power.  Beach AvDD Analog Power ground.  Beach AvDD All Pl differential data lane 3 input (Negative).  Beach AvDD All Pl differential data lane 2 input (Positive).  Beach AvDD All Pl differential data lane 2 input (Negative).  Beach AvDD All Pl differential clock input (Positive).  Beach AvDD All Pl differential data lane 1 input (Positive).  Beach AvDD All Pl differential data lane 1 input (Positive).  Beach AvDD All Pl differential data lane 1 input (Positive).  Beach AvDD All Pl differential data lane 1 input (Positive).  Beach AvDD All Pl differential data lane 1 input (Positive).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beach AvDD All Pl differential data lane 0 input (Negative).  Beac	6	LR	Left or Right Display Control.
8 LEDK 9 AVDD Analog Power. 10 GND Power ground. 11 D3P MIPI differential data lane 3 input (Positive). 12 D3N MIPI differential data lane 3 input (Negative). 13 GND Power ground. 14 D2P MIPI differential data lane 2 input (Positive). 15 D2N MIPI differential data lane 2 input (Negative). 16 GND Power ground. 17 CLKP MIPI differential clock input (Positive). 18 CLKN MIPI differential clock input (Negative). 19 GND Power ground. 20 D1P MIPI differential data lane 1 input (Positive). 21 D1N MIPI differential data lane 1 input (Negative). 22 GND Power ground. 23 D0P MIPI differential data lane 0 input (Negative). 24 D0N MIPI differential data lane 0 input (Negative). 25 GND Power ground. Standby mode. STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	7	LEDK	I ED backlight (Cathode)
10 GND Power ground.  11 D3P MIPI differential data lane 3 input (Positive).  12 D3N MIPI differential data lane 3 input (Negative) .  13 GND Power ground.  14 D2P MIPI differential data lane 2 input (Positive).  15 D2N MIPI differential data lane 2 input (Negative) .  16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative) .  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  26 STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	8	LEDK	LLD backlight (Cathode).
11 D3P MIPI differential data lane 3 input (Positive).  12 D3N MIPI differential data lane 3 input (Negative).  13 GND Power ground.  14 D2P MIPI differential data lane 2 input (Positive).  15 D2N MIPI differential data lane 2 input (Negative).  16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative).  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative).  25 GND Power ground.  26 STBYB STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	9	AVDD	Analog Power.
12 D3N MIPI differential data lane 3 input (Negative) .  13 GND Power ground.  14 D2P MIPI differential data lane 2 input (Positive).  15 D2N MIPI differential data lane 2 input (Negative) .  16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative) .  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  STBYB STBYB "H" ,normal operation(default) STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	10	GND	Power ground.
13 GND Power ground.  14 D2P MIPI differential data lane 2 input (Positive).  15 D2N MIPI differential data lane 2 input (Negative) .  16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative) .  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	11	D3P	MIPI differential data lane 3 input (Positive).
14 D2P MIPI differential data lane 2 input (Positive).  15 D2N MIPI differential data lane 2 input (Negative) .  16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative) .  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  Standby mode.  STBYB "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	12	D3N	MIPI differential data lane 3 input (Negative) .
15 D2N MIPI differential data lane 2 input (Negative) .  16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative) .  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  26 STBYB "H" ,normal operation(default)  STBYB = "L" , timing controller, source driver will turn off, all output an High-Z.	13	GND	Power ground.
16 GND Power ground.  17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative) .  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	14	D2P	MIPI differential data lane 2 input (Positive).
17 CLKP MIPI differential clock input (Positive).  18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative) .  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	15	D2N	MIPI differential data lane 2 input (Negative) .
18 CLKN MIPI differential clock input (Negative).  19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative).  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative).  25 GND Power ground.  26 STBYB STBY	16	GND	Power ground.
19 GND Power ground.  20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative).  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative).  25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	17	CLKP	MIPI differential clock input (Positive).
20 D1P MIPI differential data lane 1 input (Positive).  21 D1N MIPI differential data lane 1 input (Negative).  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative).  25 GND Power ground.  26 STBYB = "H" ,normal operation(default)  STBYB = "L" , timing controller, source driver will turn off, all output an High-Z.	18	CLKN	MIPI differential clock input (Negative).
21 D1N MIPI differential data lane 1 input (Negative).  22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative).  25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	19	GND	Power ground.
22 GND Power ground.  23 D0P MIPI differential data lane 0 input (Positive).  24 D0N MIPI differential data lane 0 input (Negative) .  25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default)  STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	20	D1P	MIPI differential data lane 1 input (Positive).
DOP MIPI differential data lane 0 input (Positive).  DON MIPI differential data lane 0 input (Negative).  GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default)  STBYB = "L" , timing controller, source driver will turn off, all output an High-Z.	21	D1N	MIPI differential data lane 1 input (Negative) .
24 D0N MIPI differential data lane 0 input (Negative).  25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	22	GND	Power ground.
25 GND Power ground.  Standby mode.  STBYB = "H" ,normal operation(default)  STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	23	D0P	MIPI differential data lane 0 input (Positive).
Standby mode.  STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	24	D0N	MIPI differential data lane 0 input (Negative) .
STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output ar High-Z.	25	GND	Power ground.
	26	STBYB	STBYB = "H" ,normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output are
Global reset pin. Active low to enter reset state.  27 RESET Suggest to connecting with an RC reset circuit for stability.  Normally pull high.(R=10KΩ, C=1μF)	27	RESET	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability.
28 VDD1.8 Digital Power 1.8V.	28	VDD1.8	Digital Power 1.8V.
29 VDD1.8 Digital Power 1.8V.	29	VDD1.8	Digital Power 1.8V.
30 VCOM Common Voltage.	30	VCOM	Common Voltage.



Version: A

2024-06-13

5. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	VDD	-0.5	1.89	V
Analog Supply Voltage	AVDD	-0.5	15	V
High Supply Voltage	VGH	-0.3	40	V
Low Supply Voltage	VGL	-20	0.3	V
Operating Temperature	Тор	-20	70	°C
Storage Temperature	Тѕт	-30	80	°C

### 6. DC Characteristics

,, 20 011d1 d0101101100							
Item	Symbol	Min.	Тур.	Max.	Unit	Remark	
Input signal Voltage	VCOM	3.0	3.6	5.0	٧	1	
Logic Supply Voltage	VDD	1.71	1.8	1.89	V		
Analog Supply Voltage	AVDD	8.9	9.7	10.5	V		
Low Supply Voltage	VGL	-7.1	-6.0	-5.5	V	-	
High Supply Voltage	VGH	16	18	19	V		
Output High Voltage	VIH	0.7XVDD	-	VDD	V	-	
Output Low Voltage	VIL	0	-	0.3xVDD	V	-	

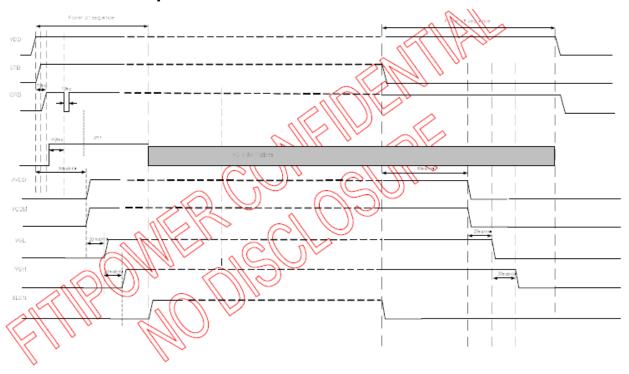
Note 1: Please adjust VCOM to make the flicker level be minimum. Typ VCOM 电压值只做参考, 具体以实际效果为准(根据FLICKER 状态可调整)

Version: A

2024-06-13

## 7. Timing Characteristics

## 7.1 Power ON/OFF Sequence



Note: CLK and Data Lanes should keep in LP11(stop state) before GRB.



Version: A

2024-06-13

## 7.2 Input Signal Timing

### 7.2.1 Basic DC Characteristic

(VDD=VDD\_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND\_IF=0V)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	>
High level input voltage	Vih	For the digital circuit	0.7×VDD	Pa	VDD	٧
Input leakage current	li	For the digital circuit	-//		∕ ±1	μΑ
High level output voltage	Voh	loh= -400 μA	VDD - 0.4	Mr. o.	-	٧
Low level output voltage	Vol	lol= +400 μA		-	GND+0.4	٧
Pull low/high resistor	Ri	For the digital input pin  VDD_IF=1.8V	200K	250K	300K	ohm
Digital Operation current	ldd	Fclk=51.2MHz, VDD=VDD_IF=1.8V		TBD	-	mA
Digital HW Stand-by current	lst1	Clock and all functions are stopped	<u>                               </u>	50		μΑ
Analog Operating Current	ldda	No Toad, Fclk=5T.2MHz, @AVDD=13.5V,V1=13.4V, V14=0.1V	) -	10	12	mA
Analog Stand-by current	Ist2	No load, clock and all functions are stopped	-	10	50	μΑ
Input level of V1 ~ V7	Vrett	Gamma correction voltage input	0.4*AVDD	-	AVDD-0.1	V
Input level of V8 - V14	₩ref2	Gamma correction voltage input	0.1	-	0.6*AVDD	V
Output Voltage deviation	Ved1	Vo = AGND+0.1V ~ AGND+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = AGND+0.5V ~ AVDD-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = AGND+0.5V ~ AVDD-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ 1536	0.1	-	AVDD-0.1	>
Sinking Current of Outputs	IOLy	SO1 ~ 1536; Vo=0.1V v.s 1.0V , AVDD=13.5V	80	-	-	uA
Driving Current of Outputs	ЮНу	SO1 ~ 1536; Vo=13.4V v.s 12.5V , AVDD=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

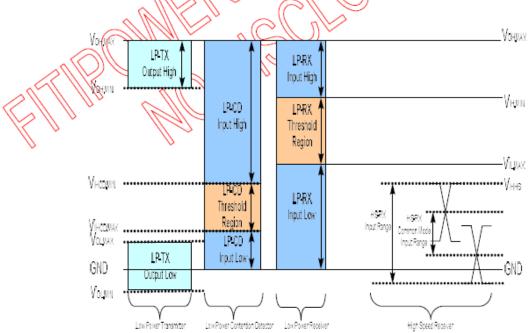
Version: A

2024-06-13

### 7.2.2 MIPI Interface DC Characteristic

(VDD=VDD\_IF=1.8V,AVDD=8 to 13.5V,GND=AGND=GND\_IF=0V,TA=-20°C to 85°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit
	MIPI Charac	teristics for High S			
Single-ended input low voltage	VILHS	-40	-	-	mV
Single-ended input high	VIHHS	-	-	460	mV
voltage					
Common-mode voltage	VCDRXDC	70	•	330	m∨
Differential input impedance	ZID		100	. 1	ohm
HS transmit differential	[Vod]	140	200	250	m∨
voltage(VOD=VDP-VDN)			$\sim$		
	MIPI Chara	acteristics for Low	Power Mode		
Pad signal voltage range	VI	-50	11/20-0	1350	mV
Ground shift	VGNDSH	-50		50	mV
Logic 0 input threshold	VIL	0		550	mV
Logic 1 input threshold	VIH	880		1350	mV
Input hysteresis	VHYST	25	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	-	mV
Output low level	Vol	-50		<u>/</u> 50	mV
Output high level	Voн	XN All	1.2//	1.3	V
Output impedance of Low	ZOLP /	$\gg$ // 80//	(//00//	125	ohm
Power Transmitter	(		$(\mathcal{C}_{\parallel})$		
Logic 0 contention threshold	VILCO, MAX	$\bigcirc$ ) - $\bigcirc$		200	mV
Logic 0 contention threshold	MINT COUNTY	4500 \\		-	mV

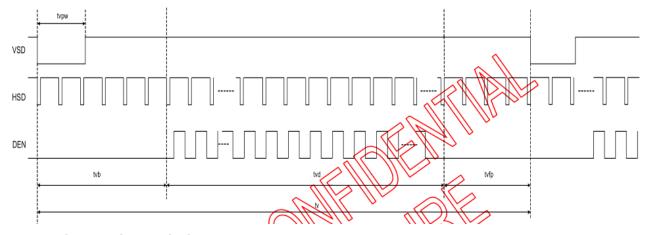


Version: A

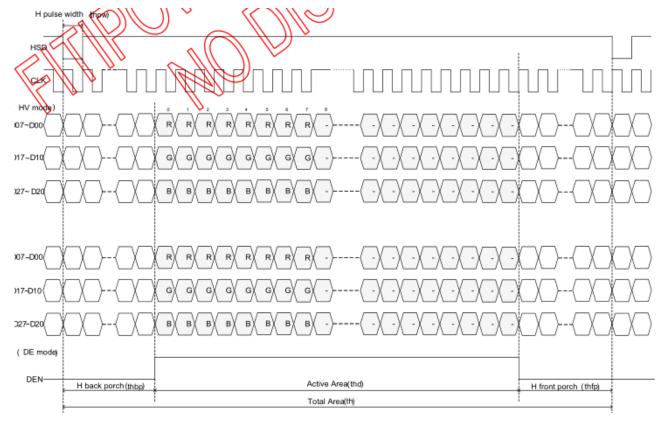
2024-06-13

### 7.2.3 Input Timing Table (4Lane)

### **Vertical input timing**



## Horizontal input timing





Version: A

2024-06-13

DE mode					
Parameter	Cumbal		Value		11.24
Parameter	Symbol	Min.	Тур.	Max.	Unit
DCLK frequency @Frame rate=60hz	fclk	40.8	51.2	67.2	Mhz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		Н
VSYNC period time	tv	610	635	800	Н
VSYNC blanking	tvb+tvfp	10	35	200	Н

HV mode Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display a	rea	thd		1024		DCLK
DCLK fraguanov@ Frama	roto-60hz	fclk	Min.	Тур.	Max.	
DCLK frequency@ Frame rate=60hz		ICIK	44.9	51.2	63	Mhz
1 Horizontal Line		th	1200	1344	1400	
	Min.		1			
HSYNC pulse width	HSYNC pulse width Typ.			_		DCLK
	Max.			140		DOLK
HSYNC back porch		thbp	160	160	160	]
HSYNC front porc	h	thfp	16	160	216	

Vertical input timing						
Parameter	Cumbal		Value	Value		
Parameter	Symbol	Min.	Тур.	Max.	Unit	
Vertical display area	tvd		600		Н	
VSYNC period time	tv	624	635	750	Н	
VSYNC pulse width	tvpw	1	_	20	Н	
VSYNC back porch	tvb	23	23	23	Н	
VSYNC front porch	tvfp	1	12	127	Н	

Version: A

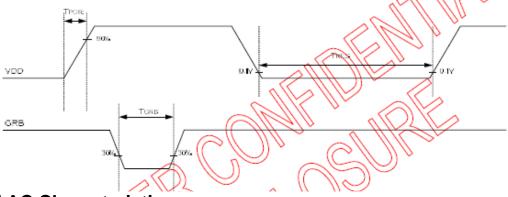
2024-06-13

#### 7.3 AC Electrical Characteristics

### 7.3.1 Basic AC Characteristic

(VDD=VDD\_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND\_IF=0V,TA=-20 to +85°C) VDD/GRB AC characteristic

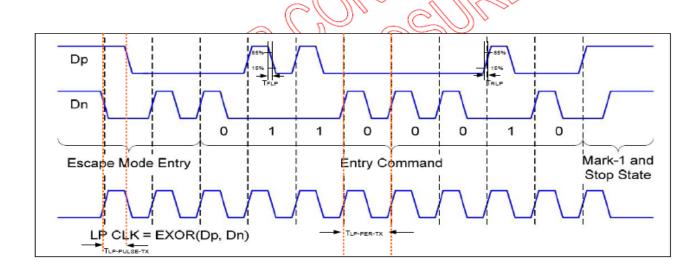
Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
VDD power slew rate	Tpor	-	-	20	ms	From 0 to 90% VDD
GRB active pulse width	TGRB	1	-	-	ms	VDD=VDD_IF=
						1.8V
VDD resettle time	Tres	1	-	-	S ^	



## 7.3.2 MIPI AC Characteristic

## **LP Transmitter AC Specification**

Parameter	Symbol	Min	Тур	Max	Units	Notes	
15%~85% risir	ng time and falling time	TRLP /TFLP	-	-	25	ns	-
30%~85% risir	ng time and falling time	Тпеот	-	-	35	ns	-
Pulse width of LP pulse after STOP state or exclusive-OR Last pulse before stop state		TLP-PULSE-TX	40	-	M. D.	ns	-
	All other pulses	1	20	- ^<	< // //	ns	-
Period of the L	P EXOR clock	TLP-PER-TX	90	7	11-110	mV/ns	-
Slew Rate @C	LOAD =0pF		30	//- \ <u>\</u>	500	mV/ns	-
Slew Rate @C	δV/δtsR	30		200	mV/ns	-	
Slew Rate @C	1	30	1111	150	mV/ns	-	
Slew Rate @C	]	30///	( )) -	100	mV/ns	-	
Load Capacita	TRLP		· -	<b>78</b>	pF	-	



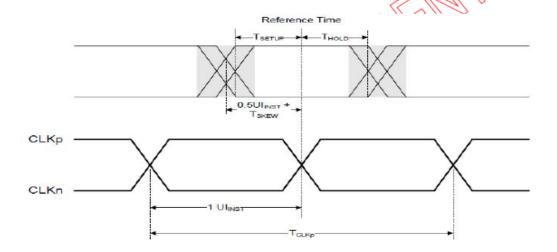


Version: A

2024-06-13

## High speed transmission

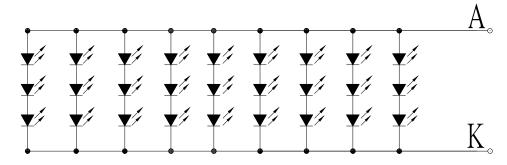
Parameter	Symbol	Min	Тур	Max	Units
UI instantaneous	Ulinst	2	-	12.5	ns
Data to Clock	Tskew(tx)	-0.15	-	0.15	Ulinst
Skew(measured at					
transmitter)					
Data to Clock Setup	TSETUP(RX)	0.15	-	-	Ulinst
time(measured at receiver)					
Data to Clock Hold	Thold(RX)	0.15	-	- 1	Ulinst
time(measured at receiver)				11 M	\
20%~80% rise time and fall	Tr, Tf	150	-		
time		-	- <	(//0.3/	Ulinst



Version: A

2024-06-13

## 8. Backlight Characteristic



Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	8.4	9.9	10.4	V	lf=160mA
Supply Current	lf	-	160	-	mA	-
Luminous Intensity for LCM	-	250	300	-	cd/m <sup>2</sup>	If=160mA
Uniformity for LCM	-	70	-	-	%	If=160mA
Life Time	-	30000	-	-	Hr	If=160mA
Backlight Color	White					



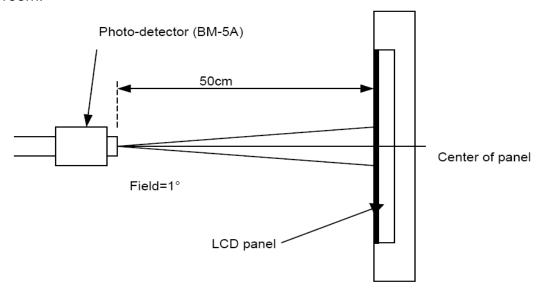
Version: A

2024-06-13

9. Optical Characteristics

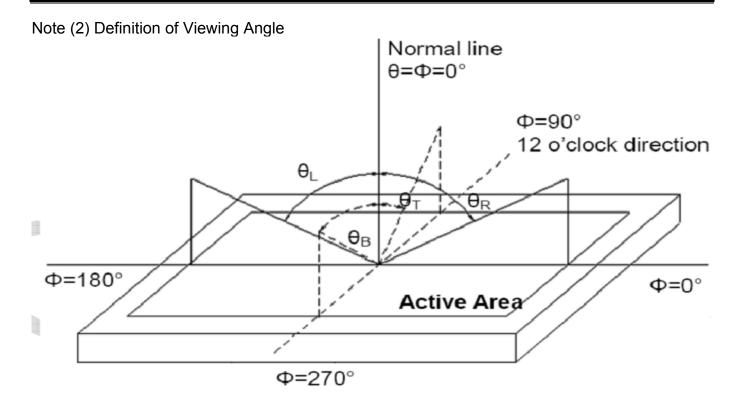
Item	Conditions		Min.	Тур.	Max.	Unit	Note	
	Horizontal	θL	ı	85	-			
Viewing Angle	HOHZOHIAI	θR	-	85	-	dograa	(1) (2) (6)	
(CR>10)	Vertical	θт	-	85	-	degree	(1),(2),(6)	
	vertical	θв	-	85	-			
Contrast Ratio	Center		600	800	-	-	(1),(3),(6)	
Dognongo Timo	Rising		28	45	mo	(1) (4) (6)		
Response Time	Falling		_	20	45	ms	(1),(4),(6)	
	Red x			TBD		-		
	Red y			TBD		-		
	Green x			TBD		-		
CF Color	Green y		Тур.	TBD	Тур.	-	(1) (6)	
Chromaticity (CIE1931)	Blue x		-0.05	TBD	+0.05	-	(1), (6)	
	Blue y	Blue y		TBD		-		
	White x			0.313		-		
	White y			0.329		-		

Note (1) Measurement Setup: The LCD module should be stabilized at given temp. 25°C for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



Version: A

2024-06-13

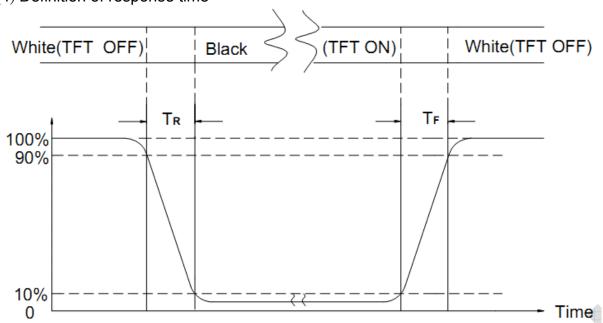


Note (3) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition of response time



Note (5) Definition of Transmittance (Module is without signal input)

Transmittance = Center Luminance of LCD / Center Luminance of Back Light x 100%

Note (6) Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD



Version: A

2024-06-13

10. Reliability Test Conditions and Methods

NO.	TEST ITEMS	TEST CONDITION					
1)	High Temperature Storage	Keep in 80°C ±5°C 96hrs					
2	Low Temperature Storage	Keep in -30°C ±5°C 96hrs					
3	High Temperature / High Humidity Storage Test	Keep in 60 ℃ / 90% R.H duration for 96hrs (Excluding the polarizer)					
4	Temperature Cycling Storage Test	$-30^{\circ}\text{C} \rightarrow +25^{\circ}\text{C} \rightarrow 80^{\circ}\text{C} \rightarrow +25^{\circ}\text{C}$ (30mins) (5mins) (30mins) (5mins) 20 Cycle					
(5)	ESD Test	Air Discharge: Apply 2 KV with 5 times Discharge for each polarity +/-  1. Temperature ambiance: $15^{\circ}\text{C} \sim 35^{\circ}\text{C}$ 2. Humidity relative: $30\% \sim 60\%$ 3. Energy Storage Capacitance( Cs + Cd ): $150\text{pF}\pm10\%$ 4. Discharge Resistance(Rd): $330\Omega\pm10\%$ 5. Discharge, mode of operation: Single Discharge (time between successive discharges at least 1 sec)  (Tolerance if the output voltage indication: $\pm5\%$ )					
6	Vibration Test (Packaged)	<ol> <li>Sine wave 10~55 Hz frequency (1 min/sweep)</li> <li>The amplitude of vibration :1.5 mm</li> <li>Each direction (X, Y, Z) duration for 2 Hrs</li> </ol>					
7	Drop Test (Packaged)	Packing Weight (Kg) Drop Height (cm)  0 ~ 45.4 122  45.4 ~ 90.8 76  90.8 ~ 454 61  Over 454 46  Drop  Direction: **1 corner / 3 edges / 6 sides each 1time					



Version: A

2024-06-13

### 11. Inspection Standard

### 11.1. QUALITY:

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

#### 11.1.1. INSPECTIONTOOLS AND INSTRUMENTS

Vernier calipers, film scales, multimeter, magnifying eyepiece, ND5%, luminance meter and so on.

#### 11.1.2. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM AMSON TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 TO 40 ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

#### 11.1.3. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION, A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (SAME AS MIL-STD-105E), LEVEL: II

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION, A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

#### 11.1.4. WARRANTY POLICY

AMSON WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. AMSON WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF AMSON.

#### 11.2. CHECKING CONDITION

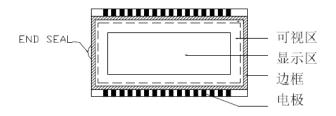
- **11.2.1.**CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.
- **11.2.2.**CHECKER SHALL SEE OVER 300±25 mm. WITH BARE EYES FAR FROM SAMPLE **11.2.3.**Ambient Illumination:

0 ~30 Lux for functional inspection

500 ~ 1200 Lux for external appearance inspection.

**11.2.4.** TEST AREA:

**11.2.5.** Inspection should be carried out with rope electrostatic ring and static finger cover (both hands except small fingers must be worn)





Version: A

2024-06-13

- **11.2.6.** The inspector may make a visual inspection or a comparative examination with a film ruler and a magnifying eyepiece. Individual defects shall be determined according to the limited samples.
- **11.2.7.** Functional testing uses electrical testing fixtures or test fixtures required by customers.
- **11.2.8.** the ion fan should be used when testing.

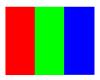
### 11.2.9. the principle of judgment

11.3.1 If the defect outside the visual area does not affect the assembly and display, it will be judged as a good product.

#### 11.3.2 Poor definition

Pixel:

A combination of three sub-pixels (Red + Green + Blue).



#### Dot:

Any of the sub-pixels (Red or Green or Blue).







### **Bright and dark dots:**

A point pixel (sub-pixel: R, G, B pixels) is lit or turned off during the display function test. **Highlights**:

Usually considered to be shown on a black screen.

### Dark spots:

They are generally considered to be shown on R, G, B solid colors or white images.

## Neighborhood:

Two or three adjacent point pixels (dot: sub-pixel) connected together (R, G or G, B or B, R or RGB).



Version: A

2024-06-13

### 11.3. INSPECTION PLAN:

	T T		
CLASS	ITEM	JUDGEMENT	CLASS
DA OLUMO A	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO.", "LOT NO." AND "QUANTITY"	Minor
PACKING &		SHOULD INDICATE ON THE PACKAGE.	
INDICATE	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXEDREJECTED	Critical
		QUANTITY SHORT OR OVERREJECTED	
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON	Major
		THE PRODUCT	
	4. DIMENSION,	ACCORDING TO SPECIFICATION OR	
ASSEMBLY	LCD GLASS SCRATCH	DRAWING.	Major
	AND SCRIBE DEFECT.		
	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE	Minor
		IS VISABLE IN THE VIEWING AREA	
		REJECTED	
	6. BLEMISH - BLACK SPOT -	ACCORDING TO STANDARD OF VISUAL	Minor
	WHITE SPOT IN THE LCD	INSPECTION(INSIDE VIEWING AREA)	
	AND LCD GLASS CRACKS		
	7. BLEMISH - BLACK SPOT	ACCORDING TO STANDARD OF VISUAL	Minor
APPEARANCE	WHITE SPOT AND SCRATCH	INSPECTION(INSIDE VIEWING AREA)	
	ON THE POLARIZER	,	
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL	Minor
		INSPECTION(INSIDE VIEWING AREA)	
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR ( OR NEWTON	
		RING) OF LCDREJECTED.	Minor
		OR ACCORDING TO LIMITED SAMPLE	
		( IF NEEDED, AND INSIDE VIEWING AREA )	
	10. ELECTRICAL AND OPTICAL	ACCORDING TO SPECIFICATION OR	Critical
	CHARACTERISTICS	DRAWING . ( INSIDE VIEWING AREA )	
	(CONTRAST: VOP:		
	CHROMATICITY ETC )		
ELECTRICAL	11.MISSING LINE	MISSING DOT. LINE . CHARACTER	Critical
		REJECTED	
	12.SHORT CIRCUIT	NO DISPLAY - WRONG PATTERN	Critical
	WRONG PATTERN DISPLAY	DISPLAY · CURRENT CONSUMPTION	
		OUT OF SPECIFICATION REJECTED	
	13. DOT DEFECT (FOR COLOR AND TFT)	ACCORDING TO STANDARD OF VISUAL	Minor



Version: A

2024-06-13

## 11.4. STANDARD OF VISUAL INSPECTION

NO.	CLASS	ITEM		JUI	OGEMENT
			(A) ROUN	ND TYPE:	unit: mm
			DIA	METER (mm.)	ACCEPTABLE Q'TY
		BLACK AND WHITE		Ø≤ <b>0</b> .2	Disregard ≥ 1mm
44.4.4	MINOR	SPOT FOREIGN INOR MATERIEL DUST IN		2 < ∅ ≤ 0.4	3 (Distance ≥ 15mm)
11.4.1		THE CELL	0.4	<b>1</b> < Ø	0
		BLEMISH SCRATCH	NOT	E: ∅=(LENGTH*W	IDTH)/2
			(S) LINEA	AR TYPE:	unit: mm
			LENGTH		ACCEPTABLE QTY
				W≤ 0.05	Disregard ≥ 1mm
			L ≤4.0	$0.05 < W \le 0.07$	
				0.07 < W	FOLLOW ROUND TYPE
		DUDDU			unit: mm.
11.4.2	MINOR	BUBBLE IN POLARIZER		DIAMETER	ACCEPTABLE Q'TY
		DENT ON		Ø<0.2	Disregard ≥ 1mm
		POLARIZER		0.2<∅≤ 0.5	2(Distance≥ 15mm)
				0.5<Ø	0
			lt.	ems	ACC. Q'TY
			Bri	ght dot	N ≤2(Distance ≥ 15mm)
				Dark dot	N ≤2(Distance ≥ 15mm)
11.4.3	MINOR	Dot Defect	Pixel Define:  Note:  1. The definition of dot: The size of a defective dot over 1/whole dot is regarded as one defective dot.  Definition:<1/2 dot and visible by 5% ND filter  2. Bright dot: Dots appear bright and unchanged in size mount which LCD panel is displaying under black pattern.  3. Dark dot: Dots appear dark and unchanged in size in value pattern.		
11.4.4	MINOR	Mura		e through 5% ND fil necessary	Iter in 50% gray or judge by limit



Version: A

2024-06-13

NO.	CLASS	ITEM	JUDGEMENT
11.4.5	MINOR	LCD GLASS CHIPPING	X ≥ 3mm Y > S Reject
11.4.6	MINOR	LCD GLASS CHIPPING	X or Y > S Reject
11.4.7	MAJOR	LCD GLASS GLASS CRACK	Continuous burst NG Reject
11.4.8	MAJOR	LCD GLASS SCRIBE DEFECT	ACCORDING TO DIMENSION
11.4.9	MINOR	LCD GLASS CHIPPING ( ON THE TERMINAL AREA )	Y<1/2Z $Y \ge 0.5 \text{mm}_{\text{Reject}}$ $X \ge 3 \text{mm}$
11.4.10	MINOR	LCD GLASS CHIPPING ( ON THE TERMINAL SURFACE )	$Y<1/2Z$ $Y \ge 0.5 mm$ $X \ge 3 mm$
11.4.11	MINOR	LCD GLASS CHIPPING	$X\geqslant 3mm$ $Y\geqslant T\qquad \text{Reject}$ $Z\qquad \text{If touch the electrode lines,}$ the need to retain the two-thirds electrode lines



Version: A

2024-06-13

## 12. Handling Precautions

### 12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

### 12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (CI), Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Sulfur (S) from customer, Responsibility is on customer.

#### 12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or ground, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

#### 12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

### 12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.
  - Usage under the maximum operating temperature, 50%Rh or less is required.



Version: A

2024-06-13

#### 12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
   [It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

### 12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

#### 13. Precaution for Use

#### 13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

#### 13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification.
- When a new problem is arisen this is not specified in this specification.
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT and some problem is arisen in this specification due to the change.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

# 14. Packing Method TBD